

BUK7210-55B

N-channel TrenchMOS standard level FET

Rev. 01 — 11 December 2008

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using NXP High-Performance Automotive (HPA) TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- 185 °C rated
- Q101 compliant
- Standard level compatible
- Very low on-state resistance

1.3 Applications

- 12 V and 24 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

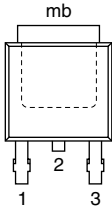
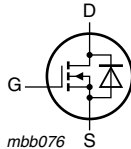
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 185\text{ °C}$	-	-	55	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3 ;	[1]	-	75	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 10 ; see Figure 9	-	8.5	10	mΩ
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\text{ Ω}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped inductive load	-	-	173	mJ

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT428 (SC-63; DPAK)</p>	 <p><i>mbb076</i></p>
2	D	drain [1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2 of the SOT428 package.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK7210-55B	SC-63; DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

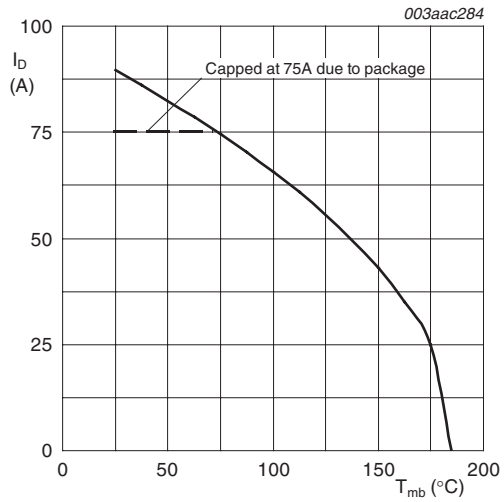
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 185\text{ °C}$	-	55	V	
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$; $25\text{ °C} \leq T_j \leq 185\text{ °C}$	-	55	V	
V_{GS}	gate-source voltage		-20	20	V	
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; see Figure 3 ;	[1]	-	89.6	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	65.5	A	
		$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; see Figure 3 ;	[2]	-	75	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed	-	335	A	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	167	W	
T_{stg}	storage temperature		-55	185	°C	
T_j	junction temperature		-55	185	°C	
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$;	[2]	-	75	A
		$T_{mb} = 25\text{ °C}$;	[3]	-	89.6	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	335	A	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped inductive load	-	173	mJ	

[1] Current is limited by power dissipation chip rating.

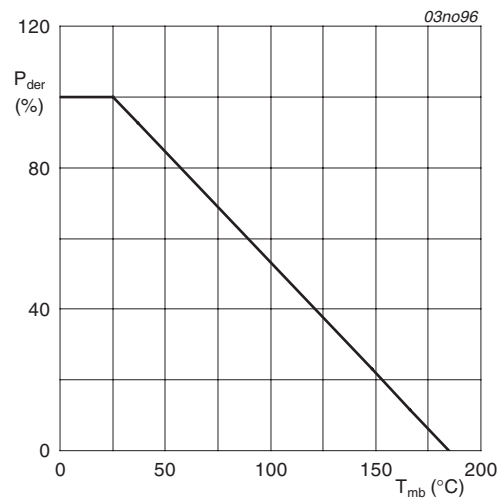
[2] Continuous current is limited by package.

[3] Current is limited by power dissipation chip rating.



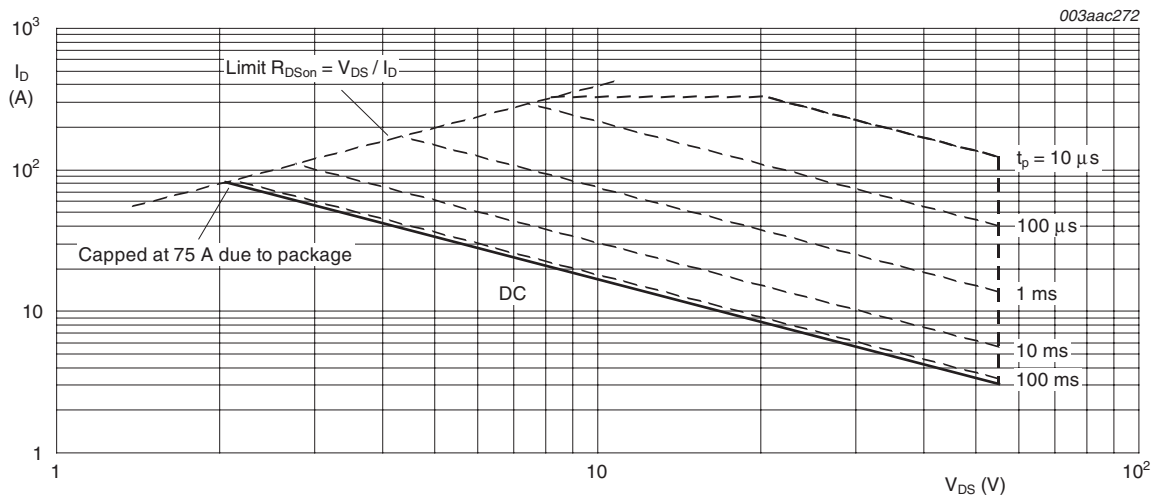
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^\circ\text{C}; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.95	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Mounted on a printed circuit board; vertical in still air.; minimum footprint	-	75	-	K/W

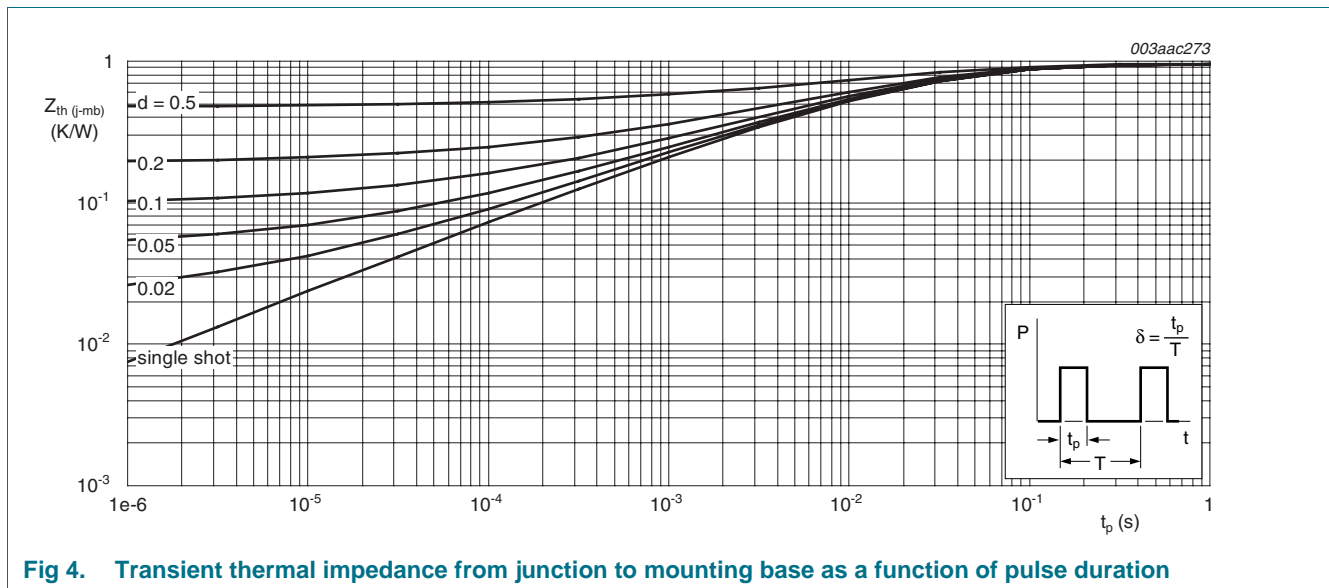


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

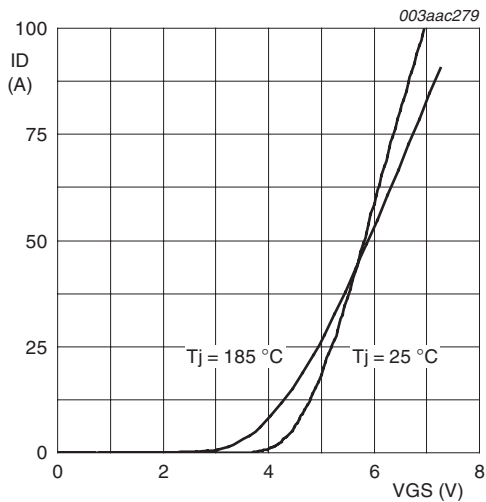
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C}$; see Figure 7	-	1.75	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$; see Figure 7 ; see Figure 8	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 185 \text{ }^\circ\text{C}$; see Figure 7	0.9	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -40 \text{ }^\circ\text{C}$; see Figure 7	-	2.8	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$; see Figure 7	-	-	4.4	V
I_{DSS}	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	1.5	500	μA
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	0.1	90	μA
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 185 \text{ }^\circ\text{C}$	-	3	800	μA
I_{GSS}	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 185 \text{ }^\circ\text{C}$; see Figure 9	-	-	20.8	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$; see Figure 10 ; see Figure 9	-	8.5	10	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 44 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$; see Figure 12 ; see Figure 13	-	35	-	nC
Q_{GS}	gate-source charge		-	9	-	nC
Q_{GD}	gate-drain charge		-	12	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$; see Figure 14	-	1840	2453	pF
C_{oss}	output capacitance		-	379	455	pF
C_{rss}	reverse transfer capacitance		-	165	226	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 25 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	18	-	ns
t_r	rise time		-	91	-	ns
$t_{d(off)}$	turn-off delay time		-	48	-	ns
t_f	fall time		-	45	-	ns
L_D	internal drain inductance	measured from drain to center of die; $T_j = 25 \text{ }^\circ\text{C}$	-	2.5	-	nH
L_S	internal source inductance	measured from source lead to source bond pad; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH

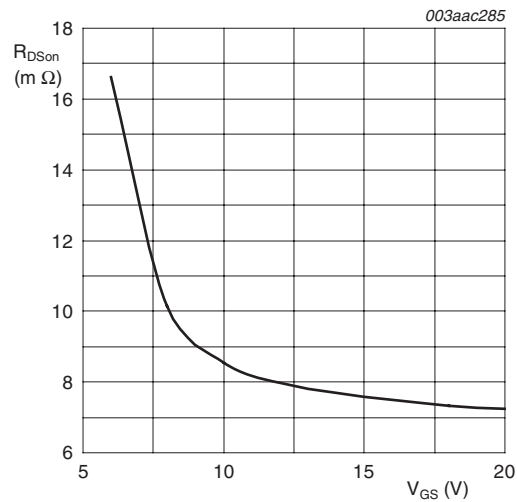
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 18\text{ A}; V_{GS} = 0\text{ V}; T_j = 150\text{ }^\circ\text{C}$	-	0.76	-	V
		$I_S = 18\text{ A}; V_{GS} = 0\text{ V}; T_j = 175\text{ }^\circ\text{C}$	-	0.74	-	V
		$I_S = 18\text{ A}; V_{GS} = 0\text{ V}; T_j = 100\text{ }^\circ\text{C}$	-	0.8	-	V
		$I_S = 18\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$; see Figure 11	-	0.85	1.2	V
		$I_S = 18\text{ A}; V_{GS} = 0\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.78	-	V
		$I_S = 18\text{ A}; V_{GS} = 0\text{ V}; T_j = 185\text{ }^\circ\text{C}$; see Figure 11	-	0.73	-	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = -10\text{ V}$	-	67	-	ns
Q_r	recovered charge	$V_{DS} = 30\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	65	-	nC



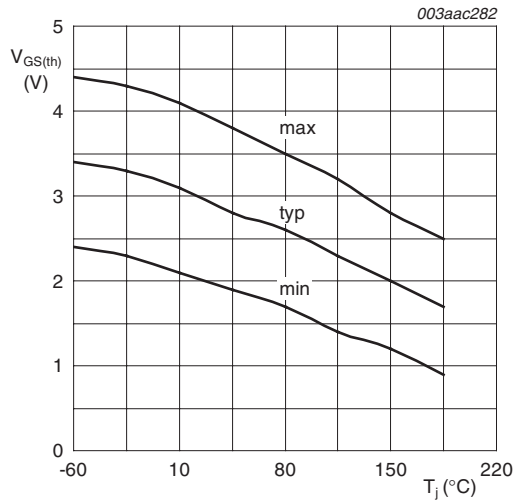
$$V_{DS} > I_D \times R_{DSon}$$

Fig 5. Transfer characteristics: drain current as a function of gate-source voltage; typical values



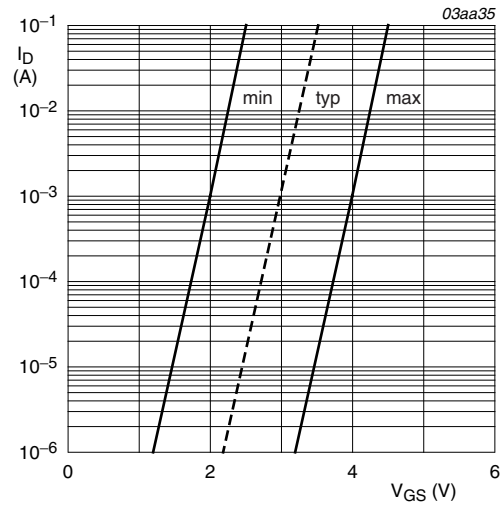
$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 25\text{ V}$$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



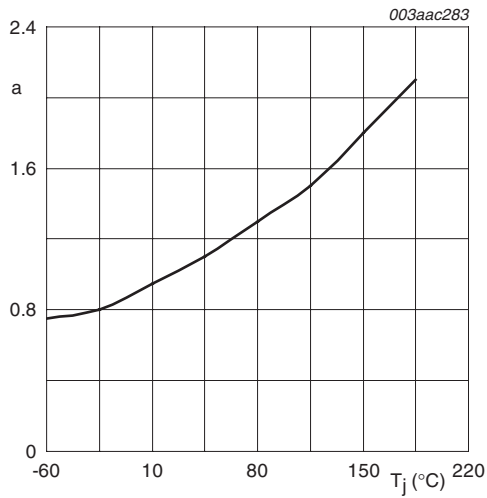
$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

Fig 7. Gate-source threshold voltage as a function of junction temperature



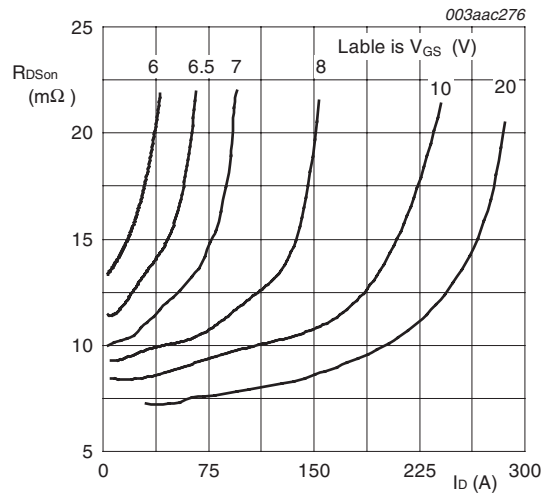
$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



$$T_j = 25\text{ }^\circ\text{C}$$

Fig 10. Drain-source on-state resistance as a function of drain current; typical values

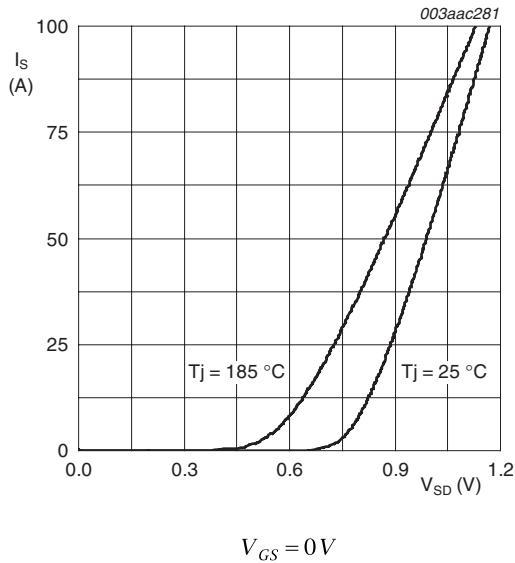


Fig 11. Source current as a function of source-drain voltage; typical values

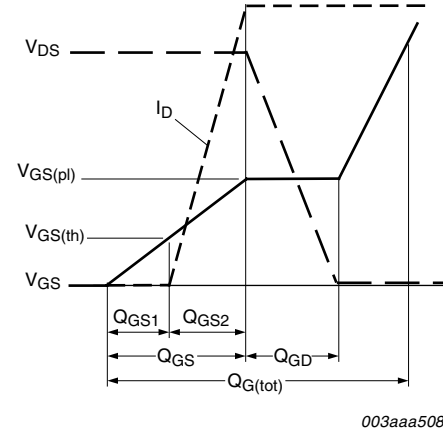


Fig 12. Gate charge waveform definitions

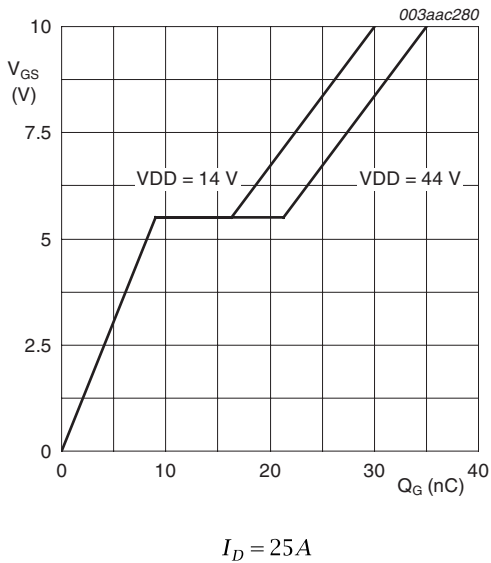


Fig 13. Gate-source voltage as a function of gate charge; typical values

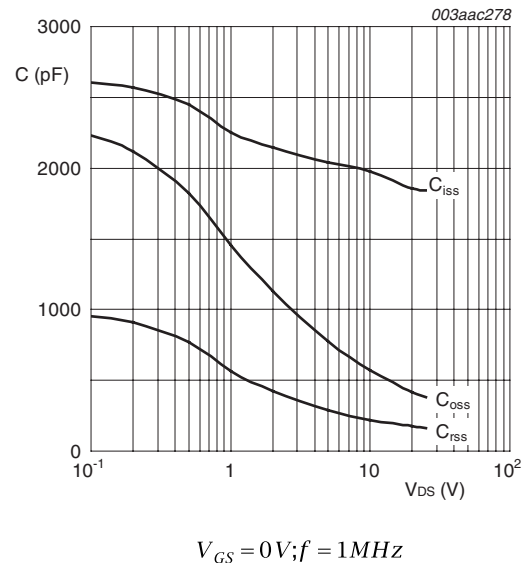


Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

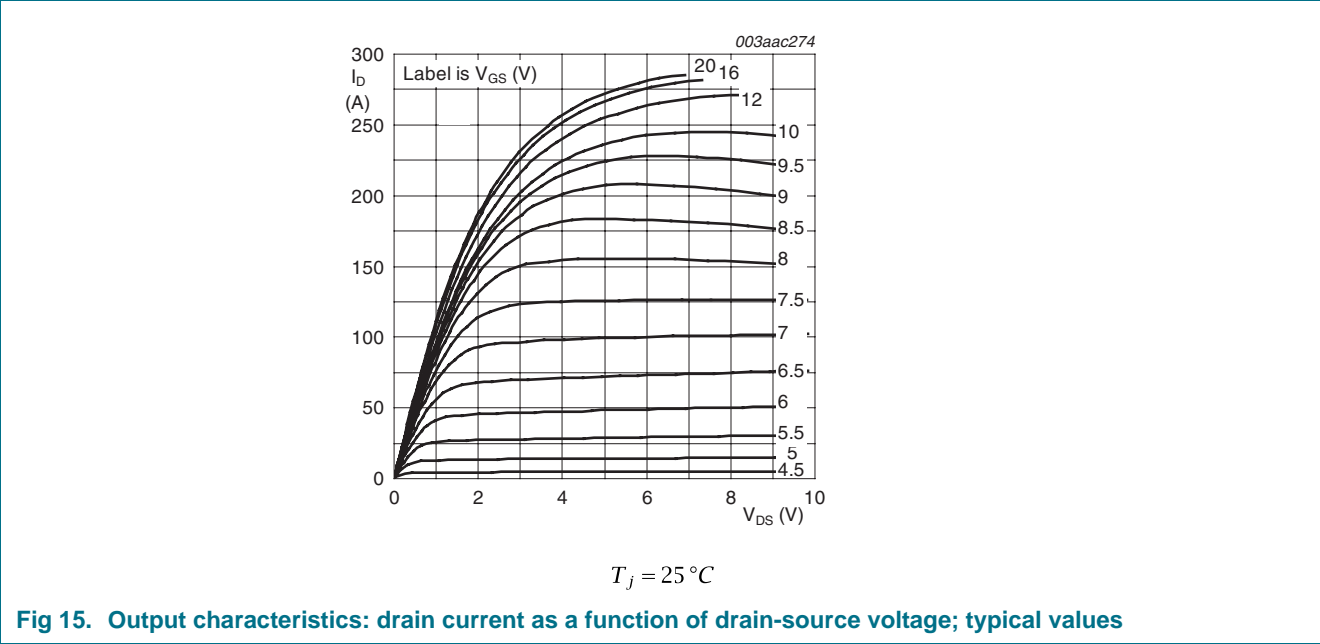


Fig 15. Output characteristics: drain current as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

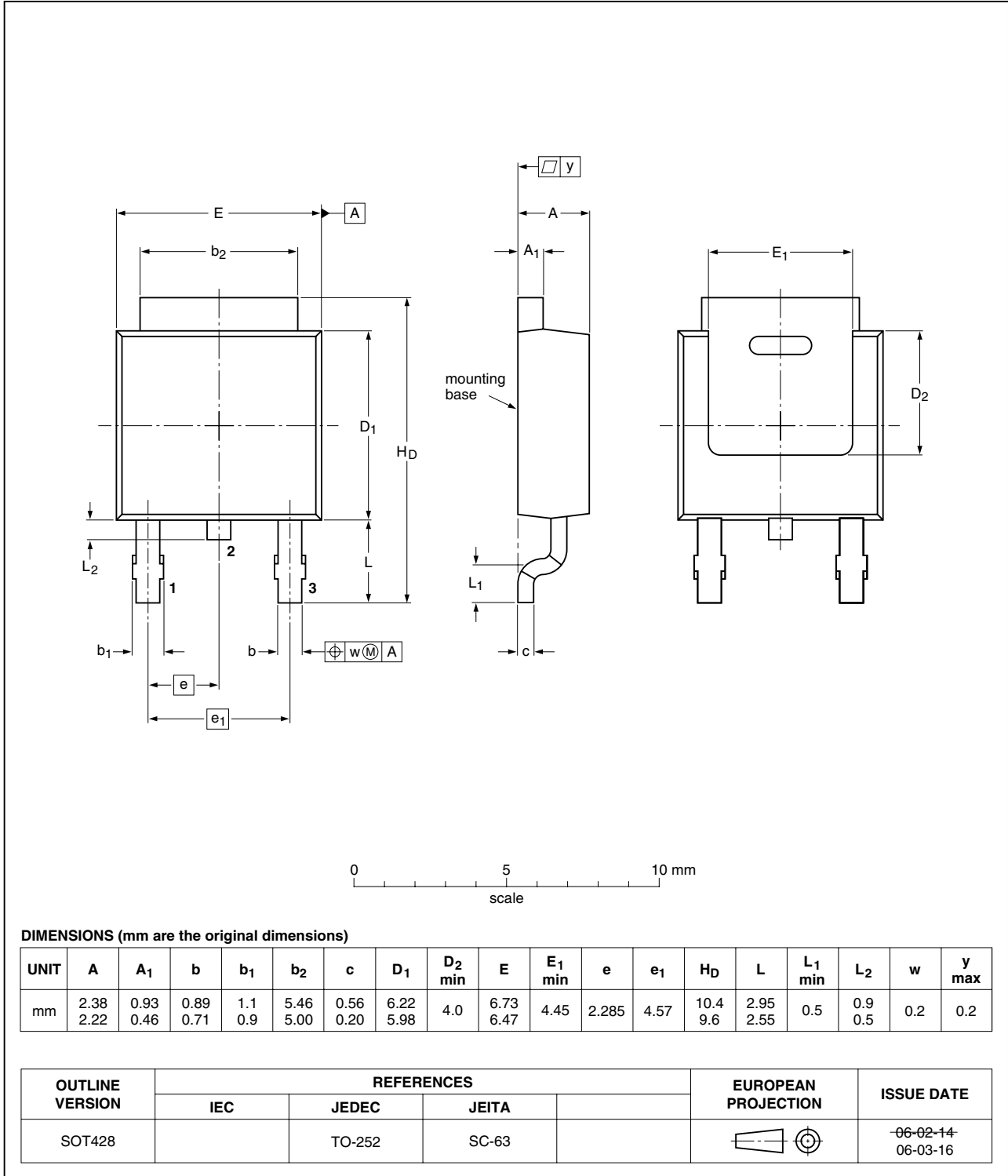


Fig 16. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7210-55B_1	20081211	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

9.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

9.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

TrenchMOS — is a trademark of NXP B.V.

10. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

11. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	3
5	Thermal characteristics	5
6	Characteristics	6
7	Package outline	11
8	Revision history	12
9	Legal information	13
9.1	Data sheet status	13
9.2	Definitions	13
9.3	Disclaimers	13
9.4	Trademarks	13
10	Contact information	13

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2008.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 11 December 2008

Document identifier: BUK7210-55B_1